



PCI/PXI acquisition card



Hardware index of PCI / PXI acquisition card

PCI and PXI cards are compatible, and the indicators are similar, two different products with same indicators and different interface are formed. According to different AD sampling rate, 14 different products are made. Indicators are listed below:

PCI card

Sampling rate	Highest 204.8K, programming controlled dividing set downward	Highest 2M, programming controlled dividing set downward	Highest 5MSPS, programming controlled dividing set downward	Highest 10MSPS, programming controlled dividing set downward	Highest 100MSPS, programming controlled dividing set downward	Highest 200MSPS, programming controlled dividing set downward	Highest 500MSPS, programming controlled dividing set downward
AD resolution	24bit	16bit	16bit	16bit	14bit	12bit	12bit
Number of input channels	2	4	4	4	4	2	2
Signal input	voltage Input or input of ICP sensors and TEDS sensor, single-ended or differential, programmable set	SMB single-ended bipolar input					
Range	$\pm 30V$ 、 $\pm 20V$ 、 $\pm 10V$ 、 $\pm 5V$ 、 $\pm 2V$ 、 $\pm 1V$ 、 $\pm 100mV$ 、 $\pm 10mV$, programmable set	$\pm 20V$ 、 $\pm 10V$ 、 $\pm 4V$ 、 $\pm 2V$ 、 $\pm 1V$ 、 $\pm 500mV$ 、 $\pm 200mV$ 、 $\pm 100mV$, programmable set				$\pm 10V$ 、 $\pm 5V$ 、 $\pm 2V$ 、 $\pm 1V$ programmable set	
Coupling	DC, AC, ground						
Trigger	Automatic trigger, analog trigger signal, external trigger						
Onboard cache	64MB	64MB	64MB	2GB	2GB	2GB	2GB
Output interface	8 DIO digital input / output, 2 DA output: Output voltage range $\pm 10V$, the sampling rate 100KSPS						
Expand	Synchronous expansion interface of multi-cards						



PXI card

Sampling rate	Highest 204.8K, programming controlled dividing set downward	Highest 2M, programming controlled dividing set downward	Highest 5Msps, programming controlled dividing set downward	Highest 10Msps, programming controlled dividing set downward	Highest 100Msps, programming controlled dividing set downward	Highest 200Msps, programming controlled dividing set downward	Highest 500Msps, programming controlled dividing set downward
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